AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Canceled).

6. (Currently Amended) ~~The memory of claim 5, wherein~~ A memory comprising: a plurality of systolic memory arrays each divided into banks, each of the memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays ~~that are divided into the plurality of banks~~ to support pipeline access to the corresponding banks using a plurality of data pipes ~~that interface with the plurality of memory arrays~~.

7. (Currently Amended) The memory of claim 6, wherein at least one of the plurality of data ~~pipe~~ pipes is used for a reading operation.

8. (Currently Amended) The memory of claim 6, wherein at least one of the plurality of data ~~pipe~~ pipes is used for a writing operation.

9. (Currently Amended) The memory of claim 6, ~~wherein there are~~ each of the plurality of systolic memory arrays includes at least eight banks ~~in each array~~.

10. (Original) The memory of claim 6, wherein a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate.

11. (Currently Amended) The memory of claim 6, wherein a clock frequency and a data path width for the pipeline architecture is determined.

12. (Currently Amended) The memory of claim 6, wherein a number of pipeline stages ~~is related~~ relates to a number of clock cycles.

13. (Original) The memory of claim 12, wherein the number of pipeline stages is the same as the number of clock cycles.

14. (Currently Amended) The memory of claim 6, wherein ~~the pipelined~~ each of the plurality of systolic memory ~~array~~ arrays is divided into a horizontal arrangement.

15. (Currently Amended) The memory of claim 6, wherein ~~the pipelined~~ each of the plurality of systolic memory ~~array~~ arrays is divided into a vertical arrangement.

16. (Original) The memory of claim 6, wherein a writing operation into memory is performed by pumping an address with data that is to be written into memory.

17. (Currently Amended) The memory of claim 6, wherein a read operation from memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks of one of the systolic memory arrays one cycle at a time.

18. (Currently Amended) The memory of claim 6, wherein memory operations from different banks having different memory addresses of one of the systolic memory arrays are interleaved.

19. (Currently Amended) The memory of claim 6, wherein ~~all~~ peripheral access for one systolic memory array is accomplished from one side of ~~a~~ the one systolic memory array.

20. (Original) The memory of claim 6, wherein whenever a bank receives a read address, memory access is initiated.

21. (Original) The memory of claim 6, wherein access latency for a bank is represented by 2i + L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

22. (Original) The memory of claim 21, wherein it will take i cycles to allow data to come out of the i th bank through a read pipeline.

23. (Original) The memory of claim 21, wherein to avoid memory collisions among data, a second read access of consecutive reads delays the placement of read result on the read data pipeline by a specified idle time.

24. (Original) The memory of claim 23, wherein the specified idle time is at least one clock cycle.

25. (Currently Amended) A processing system comprising:

a die including a microprocessor;

peripheral equipment coupled to the processing system;

~~communication channels and paths;~~

a network interface; and

on-die ~~and~~ or off-die ~~storage media wherein said storage media is a~~ systolic memory ~~array~~, the systolic memory including:

a plurality of separate systolic memory arrays, each memory array including a plurality of memory banks in a pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion.

26. (Canceled).

27. (New) The processing system of claim 25, wherein the systolic memory further comprises:

a plurality of pipeline registers, each register coupled to one of the separate systolic memory arrays.

28. (New) The processing system of claim 25, wherein each bank is associated with a mechanism to support addressing and data operations.

29. (New) The processing system of claim 25, wherein a read operation from memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks one cycle at a time.

30. (New) The processing system of claim 25, wherein access latency for a bank is represented by 2i + L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

31. (New) The memory of claim 6, further comprising:

a plurality of pipeline registers, each register to couple to one of the plurality of systolic memory arrays.

32. (New) The memory of claim 31, wherein each register is coupled to one end of a corresponding one of the systolic memory arrays.

33. (New) The memory of claim 31, wherein each register is coupled to a first one of the banks arranged in the pipelined architecture of a corresponding one of the memory arrays.

34. (New) The memory of claim 6, wherein each bank is associated with a mechanism to support addressing each data operations of the corresponding bank.

35. (New) A memory comprising:

a plurality of separate systolic memory arrays, each memory array including a plurality of memory banks in pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion.

36. (New) The memory of claim 35, further comprising:

a plurality of pipeline registers, each register to couple to one of the separate systolic memory arrays.

37. (New) The memory of claim 35, wherein each bank is associated with a mechanism to support addressing and data operations.

38. (New) The memory of claim 35, wherein a read operation is performed by pumping an address and allowing the address to flow through the address line to reach individual banks of one of the plurality of separate systolic memory arrays one cycle at a time.

39. (New) The memory of claim 35, wherein access latency for one bank of one of the plurality of separate systolic memory arrays is represented by 2i + L, where i represents time it takes to allow an address to reach a desired i th bank and L represents cycles of latency to access the memory.

40. (New) The method of claim 35, wherein peripheral access for one systolic memory array is accomplished from one side of the one systolic memory array.